What is claimed is:

1. An encryption apparatus for performing encryption of plain text blocks using data encryption standard algorithm, wherein the encryption device includes an initial permutation unit, a data encryption unit having n-stage (n is an even number) pipeline structure using a first clock, a second clock and a third clock, and an inverse initial permutation unit, the encryption device comprising:

a multiplexer for selecting one of n/3 48-bit inputs;

8 S-Boxes, each for receiving 6-bit address among the selected 48-bit and outputting 4-bit data;

a demultiplexer for distributing 32-bit data from the S-Boxes to n/3 outputs; and

a controller for control the multiplexer and the demultiplexer with a fourth clock and a fifth clock,

wherein the fourth and the fifth clock are faster than the first, the second and the third clocks by n/3 times.

2. The encryption apparatus as recited in claim 1, wherein the fourth clock is an inverse signal of the fifth clock.

3. The encryption apparatus as recited in claim 2, wherein the multiplexer and the demultiplexer perform time division between n/3 input paths and between n/3 output paths, respectively, to thereby avoid data collision.